IEEE *Xplore* ®
RELEASE 2.1

Welcome United States Patent and Trademark Office

☐ Search Session History   **BROWSE**   **SEARCH**   **IEEE XPLORE GUIDE**

Fri, 2 Jun 2006, 1:21:20 PM EST

Edit an existing query or compose a new query in the Search Query Display.

Search Query Display

Select a search number (#) to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Recent Search Queries

#1   ((wire harness<sentence>design and layout and electrical<sentence>system) <in>metadata)

#2   wire harness??<sentence>design* and layout

#3   wire harness??<sentence>design* and layout

#4   wire harness??<sentence>design* and layout

#5   wire harness??<sentence>design* and layout

#6   (wire harness??<sentence>design* and rout*<IN>metadata)

Help   Contact Us   Privac

© Copyright 2006 IE

Indexed by
⬚ Inspec®

IEEE Xplore® RELEASE 2.1

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for "wire harness??<sentence>design* and layout"

✉ e-mail

Your search matched 4 of 1351415 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History

New Search

Modify Search

wire harness??<sentence>design* and layout	Search >

☐ Check to search only within this results set

Display Format: ● Citation   ○ Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items   Select All Deselect All

☐ 1. **WHEELS: a statistical approach to EMC model validation**
Jennings, P.; Ball, R.; Lever, P.; Macdonald-Bradley, C.; Baker, S.;
Electromagnetic Compatibility, 1998. 1998 IEEE International Symposium on
Volume 2, 24-28 Aug. 1998 Page(s):1178 - 1182 vol.2
Digital Object Identifier 10.1109/ISEMC.1998.750376

AbstractPlus | Full Text: PDF(424 KB)   IEEE CNF
Rights and Permissions

☐ 2. **Future trends in EMC testing of automotive systems**
Young, P.;
Electromagnetic Compatibility for Automotive Electronics (Ref. No. 1999/134), IEE Seminar on
28 Sept. 1999 Page(s):1/1 - 1/5

AbstractPlus | Full Text: PDF(200 KB)   IEE CNF

☐ 3. **CADCAM wiring applications: using mechanical CADCAM systems for wiring**
Billsdon, R.;
Computing & Control Engineering Journal
Volume 6, Issue 1, Feb. 1995 Page(s):49 - 53

AbstractPlus | Full Text: PDF(320 KB)   IEE JNL

☐ 4. **Innovation to reality - introducing state-of-the-art protection and monitoring to existing low-**
Reber, S.; Pintar, M.; Eaves, C.;
Cement Industry Technical Conference, 2004. IEEE-IAS/PCA
25-30 April 2004 Page(s):29 - 39

AbstractPlus | Full Text: PDF(779 KB)   IEEE CNF
Rights and Permissions

Help   Contact Us   Privac

IEEE *Xplore*®
RELEASE 2.1

Welcome United States Patent and Trademark Office

□ Search Results   BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for "(wire harness??<sentence>design* and rout*<in>metadata)"   ✉ e-mail
Your search matched 1 of 1351415 documents.
A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

View Session History   **Modify Search**

New Search   (wire harness??<sentence>design* and rout*<in>metadata)   **Search** ⟩

                                     ☐ Check to search only within this results set

» Key   **Display Format:**   ◉ Citation   ○ Citation & Abstract

IEEE JNL   IEEE Journal or Magazine

IEE JNL   IEE Journal or Magazine   **view selected items**   Select All Deselect All

IEEE CNF   IEEE Conference Proceeding

IEE CNF   IEE Conference Proceeding   ☐   1. **CADCAM wiring applications: using mechanical CADCAM systems for wiring**
                                                 Billsdon, R.;
IEEE STD   IEEE Standard   Computing & Control Engineering Journal
                                                 Volume 6, Issue 1, Feb. 1995 Page(s):49 - 53

                                                 AbstractPlus | Full Text: PDF(320 KB)   IEE JNL

Indexed by
Inspec®

P🅰RTAL

USPTO

Search: ⦿ The ACM Digital Library   ○ The Guide

wire harness<sentence>design* and layout   **SEARCH**

THE ACM DIGITAL LIBRARY

🔖 Feedback Report a problem Satisfaction survey

Terms used <u>wire</u> <u>harness</u> <u>sentence</u> <u>design</u> and <u>layout</u>   Found **3,875** of **177,263**

| Sort results by | relevance ▼ |
| Display results | expanded form ▼ |

💾 Save results to a Binder
❓ Search Tips
☐ Open results in a new window

Try an <u>Advanced Search</u>
Try this search in <u>The ACM Guide</u>

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10   next
Best 200 shown   Relevance scale ☐▭▬■■

1   On driving many long wires in a VLSI layout
Vijaya Ramachandran
August 1986 **Journal of the ACM (JACM)**, Volume 33 Issue 4
Publisher: ACM Press
Full text available: 📄 <u>pdf(1.13 MB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>, <u>review</u>

It is assumed that long wires represent large capacitive loads, and the effect on the area of a VLSI layout when drivers are introduced along many long wires in the layout is investigated. A layout is presented for which the introduction of standard drivers along long wires squares the area of the layout; it is shown, however, that the increase in area is never greater than the layout's area squared if the driver can be laid out in a square region. This paper also shows an ...

2   Layout-Driven SOC Test Architecture Design for Test Time and Wire Length Minimization
Sandeep Kumar Goel, Erik Jan Marinissen
March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**
Publisher: IEEE Computer Society
Full text available: 📄 <u>pdf(343.98 KB)</u>
📄 <u>Publisher Site</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>citings</u>, <u>index terms</u>

This paper extends existing SOC test architecture design approaches that minimize required tester vector memory depth and test application time, with the capability to minimize the wire length required by the test architecture. We present a simple, yet effective wire length cost model for test architectures together with a new test architecture design algorithm that minimizes both test time and wire length. The user specifies the relative weight of the costs of test time versus wire length. In a ...

3   Latency tolerance and asynchronous design: Pre-layout wire length and congestion estimation
Qinghua Liu, Malgorzata Marek-Sadowska
June 2004 **Proceedings of the 41st annual conference on Design automation**
Publisher: ACM Press
Full text available: 📄 <u>pdf(175.56 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

In this paper, we study the pre-layout wire length and congestion estimation. We find that

two structural metrics, mutual contraction and net range, can be used to predict wire lengths. These metrics have different application ranges and complement each other. We also propose a new metric, the structural pin density, to capture the peak routing congestion of designs. Larger maximum pin densities usually lead to larger peak congestions in circuits with similar average congestions. We demonstrate ...

Keywords: congestion, prediction, wire length

4　Pre-layout estimation of individual wire lengths
Srinivas Bodapati, Farid N. Najm
April 2000 **Proceedings of the 2000 international workshop on System-level interconnect prediction**
Publisher: ACM Press
Full text available: pdf(621.30 KB)　　Additional Information: full citation, references, citings, index terms

5　A wire-length minimization algorithm for single-layer layouts
De-Sheng Chen, Majid Sarrafzadeh
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society Press
Full text available: pdf(453.58 KB)　　Additional Information: full citation, references, index terms

6　Buffered Steiner tree construction with wire sizing for interconnect layout optimization
Takumi Okamoto, Jason Cong
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society
Full text available: pdf(229.77 KB)　　Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

This paper presents an efficient algorithm for buffered Steiner tree construction with wire sizing. Given a source and n sinks of a signal net, with given positions and a required arrival time associated with each sink, the algorithm finds a Steiner tree with buffer insertion and wire sizing so that the required arrival time (or timing slack) at the source is maximized. The unique contribution of our algorithm is that it performs Steiner tree construction, buffer insertion, and wire sizing simul ...

Keywords: Interconnect Optimization, Steiner Tree, Buffer Insertion, Wire Sizing

7　Advances in homotopic layout compaction
S. Gao, M. Kaufmann, F. M. Maley
March 1989 **Proceedings of the first annual ACM symposium on Parallel algorithms and architectures**
Publisher: ACM Press
Full text available: pdf(1.26 MB)　　Additional Information: full citation, index terms

8　Floorplanning and Postlayout Optimization: TEG: a new post-layout optimization method

Shuo Zhang, Wayne W.-M. Dai
April 2002 **Proceedings of the 2002 international symposium on Physical design**
Publisher: ACM Press

Full text available: pdf(240.53 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Post-layout is an important stage in modern VLSI design. With the completed detail routing, it is the only stage where extraction and verification tools can get accurate results for further optimization. But the problem is that design optimization or modification is very hard to perform in the post-layout stage, because most layout elements are under tight geometry constraints due to the routing. In this paper we propose a new method to resolve this problem, named TEG. Based on an improve ...

9 VLSI layout and packaging of butterfly networks

Chi-Hsiang Yeh, Behrooz Parhami, E. A. Varvarigos, H. Lee
July 2000 **Proceedings of the twelfth annual ACM symposium on Parallel algorithms and architectures**
Publisher: ACM Press

Full text available: pdf(358.87 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

We present a scheme for optimal VLSI layout and packaging of butterfly networks under the Thompson model, the multilayer grid model, and the hierarchical layout model. We show that when L layers of wires are available, an N-node butterfly network can be laid out with area 4N2/L2 log22 N + o (N

10 A novel VLSI layout fabric for deep sub-micron applications

Sunil P. Khatri, Amit Mehrotra, Robert K. Brayton, Ralf H. J. M. Otten, Alberto Sangiovanni-Vincentelli
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(120.64 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

11 A layout dependent full-chip copper electroplating topography model
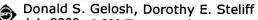
Jianfeng Luo, Qing Su, C. Chiang, J. Kawa
May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**
Publisher: IEEE Computer Society
Full text available: pdf(538.98 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>

In this paper, a layout dependent full-chip electroplating (ECP) topography model is developed based on the additive nature of the physics of the EP process. Two layout attributes: layout density, and feature perimeter sum are used to compute the post-ECP topography. Under a unified mechanism, two output variables representing the final topography: the array height and the step height are modeled simultaneously. Using the proposed model long-range effects of the ECP process can be incorporated e ...

12 Modeling layout tools to derive forward estimates of area and delay at the RTL level

Donald S. Gelosh, Dorothy E. Steliff
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES),**
Volume 5 Issue 3
Publisher: ACM Press
Full text available: pdf(278.32 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Forward estimates of area and delay facilitate effective decision-making when searching the solution space of digital designs. Current estimation techniques focus on modeling the layout result and fail to deliver timely or accurate estimates. This paper presents a novel

approach to deriving these area and delay estimates at the RTL level by modeling the layout tool, rather than the layout result. This approach uses machine learning techniques to capture the relationships between general des ...

Keywords: VLSI CAD, estimation, estimation techniques, layout, machine learning

13 <u>LIBRA—a library-independent framework for post-layout performance optimization</u>
Ric Chung-Yang Huang, Yucheng Wang, Kwang-Ting Chen
April 1998 **Proceedings of the 1998 international symposium on Physical design**
Publisher: ACM Press

Full text available: pdf(906.11 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

In this paper we present a post-layout timing optimization framework which (1) is library-independent such that it can take the logic-optimized Verilog file as its input netlist, (2) provides a prototype interface which can communicate with any vendor's physical design tools to obtain the accurate timing, topological and physical information, and perform ECO placement and routing, and (3) has fast and powerful rewiring routines that offer an extra solution space beyond the existing physical ...

14 <u>Virtual grid symbolic layout</u>
Neil Weste
June 1981 **Proceedings of the 18th conference on Design automation**
Publisher: IEEE Press

Full text available: pdf(708.40 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Free form or "stick" type symbolic layout provides a means of simplifying the design of IC subcircuits. To successfully utilize this style of layout, a complete design approach and the necessary tools to support this methodology are required. In particular, one of the requirements of such a design method is the ability to "compact" the loosely specified topology to create a set of valid mask data. This paper presents a new compaction strategy which uses the concept o ...

15 <u>Symbolic layout compaction review</u>
David G. Boyer
June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**
Publisher: IEEE Computer Society Press

Full text available: pdf(937.98 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Symbolic layout and compaction is reaching a mature status. This is demonstrated, in part, by the recent or imminent introductions of a number of commercial symbolic layout and compaction systems. The two most frequently used symbolic layout compaction approaches, constraint graph compaction and virtual grid compaction, are reviewed in this paper. The current status of these two approaches is presented by looking at the results of the ICCD87 compaction benchmark session.

16 <u>Virtual grid symbolic layout</u>
N. Weste
June 1988 **Papers on Twenty-five years of electronic design automation**
Publisher: ACM Press

Full text available: pdf(872.99 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

17 VIA minimization by layout modification

K.-S. The, D. F. Wong, J. Cong
June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(565.74 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present in this paper a new approach to the two-layer via minimization problem. Our approach is to systematically eliminate vias by modifying the routing layout. We have implemented our algorithm and applied it to benchmark routing layouts published in the literature, and obtained significant reduction in the number of vias without increasing the routing area. The experimental results show that our algorithm is more effective in via reduction and more efficient in running time compared t ...

18 Post-layout logic restructuring for performance optimization

Yi-Min Jiang, Angela Krstic, Kwang-Ting Cheng, Malgorzata Marek-Sadowska
June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**
Publisher: ACM Press

Full text available: pdf(34.50 KB)   Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

We propose a new methodology based on incrementallogic restructuring for post-layout performance improvement.The new post-layout logic restructuring techniqueallows to use accurate interconnection delays for performanceoptimization, while the incremental nature of thetechnique guarantees convergence between logic synthesisand layout. The technique can be further integrated withother post-layout optimization techniques such as gate sizingand buffer insertion. Experimental results show that thiste ...

19 Combined topological and functionality based delay estimation using a layout-driven approach for high level applications

Champaka Ramachandran, Fadi J. Kurdahi
November 1992 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press

Full text available: pdf(854.38 KB)   Additional Information: full citation, references, citings, index terms

20 Processor networks and interconnection networks without long wires (extended abstract)

Richard Beigel, Clydel P. Kruskal
March 1991 **ACM SIGARCH Computer Architecture News**, Volume 19 Issue 1
Publisher: ACM Press

Full text available: pdf(776.78 KB)   Additional Information: full citation, abstract, index terms

One processor network that is especially attractive for parallel processing is the Butterfly network. A very closely related interconnection network is the Bidelta (or Omega) network. It is well known how to lay out these networks with minimal area, but these layouts use long wires. We show how to lay them out with optimal area and short wires. We also introduce the Mesh-Connected Cycles network, which has optimal area (in the sense of AT^2) for a broad range of running times wh ...

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10   next

Useful downloads: Adobe Acrobat   QuickTime   Windows Media Player   Real Player

PØRTAL
USPTO

Search: ◉ The ACM Digital Library   ○ The Guide

wire harness<sentence>design* and rout*   **SEARCH**

THE ACM DIGITAL LIBRARY

ı꜀ Feedback Report a problem Satisfaction survey

Terms used <u>wire</u> <u>harness</u> <u>sentence</u> <u>design</u> and <u>rout</u>   Found **6,938** of **177,263**

| Sort results by | relevance ▽ |
| Display results | expanded form ▽ |

❤ Save results to a Binder
⬚ Search Tips
☐ Open results in a new window

Try an <u>Advanced Search</u>
Try this search in <u>The ACM Guide</u>

Results 1 - 20 of 200   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> <u>8</u> <u>9</u> <u>10</u>   <u>next</u>
Best 200 shown   Relevance scale ☐▱▬▮■

1 <u>Routing: Wire type assignment for FPGA routing</u>
Seokjin Lee, Hua Xiang, D. F. Wong, Richard Y. Sun
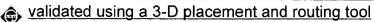February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Publisher: ACM Press
Full text available: 🔧 <u>pdf(239.36 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

The routing channels of an FPGA consist of wire segments of various types providing the tradeoff between performance and routability. In the routing architectures of recently developed FPGAs (e.g., Virtex-II), there are more versatile wire types and richer connections between them than those of the older generations of FPGAs (e.g. XC4000). To fully exploit the potential of the new routing architectures, it is beneficial to perform wire type assignment for all channels as an intermediate stage be ...

Keywords: FPGA routing, min-cost flow algorithm, wire type assignment

2 <u>Interconnect in three dimensions: A 3-D FPGA wire resource prediction model validated using a 3-D placement and routing tool</u>
Young-Su Kwon, Payam Lajevardi, Anantha P. Chandrakasan, Frank Honoré, Donald E. Troxel
April 2005 **Proceedings of the 2005 international workshop on System level interconnect prediction**
Publisher: ACM Press
Full text available: 🔧 <u>pdf(474.02 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

The interconnection architecture of FPGAs such as switches dominates performance of FPGAs. Three-dimensional integration of FPGAs overcomes interconnect limitations by allowing instances to be located and signals to be routed in 3-D space. Wire resource prediction is important for fast and accurate interconnection planning in 3-D FPGA. In this paper, we extend the existing analytic model shown in [13] with a new parameter for our 3-D FPGA which has cluster-based logic blocks. The proposed wire r ...

Keywords: 3-D FPGA, wire resource prediction

3 <u>Buffered tree construction: An efficient routing tree construction algorithm with buffer insertion, wire sizing and obstacle considerations</u>

Sampath Dechu, Zion Cien Shen, Chris C. N. Chu

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(145.28 KB)

Additional Information: full citation, abstract, references

Publisher Site

In this paper, we propose a fast algorithm to construct a performance driven routing tree with simultaneous buffer insertion and wire sizing in the presence of wire and buffer obstacles. Recently several algorithms [1, 2, 3, 4] have been published addressing the routing tree construction problem. But all these algorithms are slow and not scalable. In this paper we propose an algorithm which is fast and scalable with problem size. The main idea of our approach is to specify some important high-le ...

4 Zero-skew clock tree construction by simultaneous routing, wire sizing and buffer insertion

I-Min Liu, Tan-Li Chou, Adnan Aziz, D. F. Wong

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(218.22 KB)   Additional Information: full citation, references, citings

5 DUNE: a multi-layer gridless routing system with wire planning

Jason Cong, Jie Fang, Kei-Yong Khoo

May 2000 **Proceedings of the 2000 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(278.98 KB) Additional Information: full citation, references, citings

6 Timing-driven hierarchical global routing with wire-sizing and buffer-insertion for VLSI with multi-routing-layer

Takahiro Deguchi, Tetsushi Koide, Shin'ichi Wakabayashi

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(192.18 KB)   Additional Information: full citation, references, citings

7 Wire routing by optimizing channel assignment within large apertures

Akihiro Hashimoto, James Stevens

June 1971 **Proceedings of the 8th workshop on Design automation**

Publisher: ACM Press

Full text available: pdf(890.21 KB)   Additional Information: full citation, abstract, references, citings, index terms

The purpose of this paper is to introduce a new wire routing method for two layer printed circuit boards. This technique has been developed at the University of Illinois Center for Advanced Computation and has been programmed in ALGOL for a B5500 computer. The routing method is based on the newly developed channel assignment algorithm and requires many via holes. The primary goals of the method are short execution time and high wireability. Actual design specifications for ILLIAC IV Control ...

8 Wire routing by optimizing channel assignment within large apertures

A. Hashimoto, J. Stevens

June 1988 **Papers on Twenty-five years of electronic design automation**

Publisher: ACM Press

Full text available: pdf(1.15 MB)   Additional Information: full citation, references, index terms

9 Route packets, net wires: on-chip inteconnectoin networks

William J. Dally, Brian Towles

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(124.76 KB)   Additional Information: full citation, abstract, references, citings, index terms

Using on-chip interconnection networks in place of ad-hoc glo-bal wiring structures the top level wires on a chip and facilitates modular design. With this approach, system modules (processors, memories, peripherals, etc...) communicate by sending packets to one another over the network. The structured network wiring gives well-controlled electrical parameters that eliminate timing iterations and enable the use of high-performance circuits to reduce latency and increase bandwidth. The ar ...

10 Session 9: Routing and Clocking: Optimal minimum-delay/area zero-skew clock tree wire-sizing in pseudo-polynomial time

Jeng-Liang Tsai, Tsung-Hao Chen, Charlie Chung-Ping Chen

April 2003 **Proceedings of the 2003 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(389.93 KB)   Additional Information: full citation, abstract, references, index terms

In 21st-Century VLSI design, clocking plays crucial roles for both performance and timing convergence. Due to their non-convex nature, optimal minimum-delay/area zero-skew wire-sizing problems have long been considered intractable. None of the existing approaches can guarantee optimality for general clock trees to the authors' best knowledge. In this paper, we present an ε-optimal zero-skew wire-sizing algorithm, *ClockTune*, which guarantees zero-skew with delay and area within ε ...

Keywords: ε-optimal, clock tree, incremental refinement, pseudo-polynomial, wire-sizing, zero-skew

11 Nano and Emerging Technologies: QCA channel routing with wire crossing minimization

Brian Stephen Smith, Sung Kyu Lim

April 2005 **Proceedings of the 15th ACM Great Lakes symposium on VLSI**

Publisher: ACM Press

Full text available: pdf(155.05 KB)   Additional Information: full citation, abstract, references, index terms

Quantum-dot Cellular Automata (QCA) is a novel computing mechanism that can represent binary information based on spatial distribution of electron charge configuration in chemical molecules. QCA layout is currently restricted to a single layer with very limited number of wire crossing permitted. Thus, wire crossing minimization is crucial in improving the manufacturability of QCA circuits. In this article, we present the first QCA channel routing algorithm for wire crossing minimization. Our cha ...

Keywords: QCA channel routing, weighted minimum feedback edge set, wire crossing

minimization

12 New performance driven routing techniques with explicit area/delay tradeoff and
simultaneous wire sizing
John Lillis, Chung-Kuan Cheng, Ting-Ting Y. Lin, Ching-Yen Ho
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(346.69 KB)   Additional Information: full citation, references, citings, index terms

13 Routing through a dense channel with minimum total wire length
Michael Formann, Dorothea Wagner, Frank Wagner
March 1991 **Proceedings of the second annual ACM-SIAM symposium on Discrete
algorithms**
Publisher: Society for Industrial and Applied Mathematics
Full text available: pdf(568.63 KB)   Additional Information: full citation, references, citings, index terms

14 An optimal solution to a wire-routing problem (preliminary version)
Martin Tompa
April 1980 **Proceedings of the twelfth annual ACM symposium on Theory of
computing**
Publisher: ACM Press

Full text available: pdf(818.44 KB)   Additional Information: full citation, abstract, references, citings, index
terms

A wire-routing problem which arises commonly in the layout of circuits for very large scale
integration (VLSI) is discussed. Given the coordinates of terminals u1, u2, ..., un of one
component and v1, v2, ..., vn of another, the problem is to lay out n wires so that the ith
wire connects ui to vi, and a ...

15 Amon: a parallel slice algorithm for wire routing
Hesham Keshk, Shin-ichiro Mori, Hiroshi Nakashima, Shinji Tomita
July 1995 **Proceedings of the 9th international conference on Supercomputing**
Publisher: ACM Press
Full text available: pdf(884.02
KB)   Additional Information: full citation, references, citings, index terms

16 An efficient sequential quadratic programming formulation of optimal wire spacing for
cross-talk noise avoidance routing
Paul B. Morton, Wayne Dai
April 1999 **Proceedings of the 1999 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(857.65 KB)   Additional Information: full citation, references, citings, index terms

17 Amon2: a parallel wire routing algorithm on a torus network parallel computer
Hesham Keshk, Shin-ichiro Mori, Hiroshi Nakashima, Shinji Tomita
January 1996 **Proceedings of the 10th international conference on Supercomputing**
Publisher: ACM Press

Full text available: pdf(895.78 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

18 <u>Global wiring on a wire routing machine</u>

Ravi Nair, Se June Hong, Sandy Liles, Ray Villani
January 1982 **Proceedings of the 19th conference on Design automation**
Publisher: IEEE Press

Full text available: pdf(603.21 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

A new global wiring algorithm designed for implementation on special purpose physical design machines is described. This algorithm computes more accurate estimates of wiring channel demand and supply than other known algorithms. It also makes better use of this information in determining wire routes. By exploiting the parallel processing capability of an interconnected array of microcomputers, the global wiring is completed effectively and quickly even for large chips.

19 <u>Parallel automated wire-routing with a number of competing processors</u>

Yoshizo Takahashi, Shigetaka Sasaki
June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing ICS '90**, Volume 18 Issue 3b
Publisher: ACM Press

Full text available: pdf(718.03 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

The purpose of the automated wire routing for VLSI and printed circuit board design is to connect a number of terminal pairs distributed throughout wiring plane with net paths which do not intersect each other. Although maze running and line search are well known algorithms used for this purpose, they need a considerable computing time. To reduce it we have developed a new parallel routing algorithm in which a number of processors compete in wiring different nets independent of each other, ...

20 <u>Global wiring on a wire routing machine</u>

R. Nair, S. J. Hong, S. Liles, R. Villani
June 1988 **Papers on Twenty-five years of electronic design automation**
Publisher: ACM Press
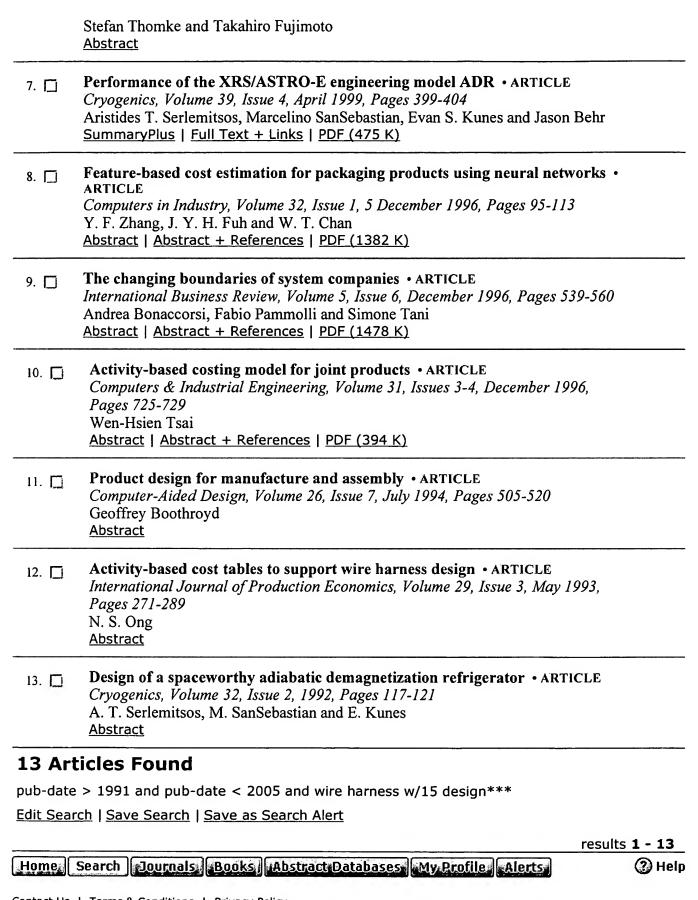
Full text available: pdf(733.41 KB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>index terms</u>

Results 1 - 20 of 200   Result page: **1** <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> <u>8</u> <u>9</u> <u>10</u>   <u>next</u>

Home | Search | Journals | Books | Abstract Databases | My Profile | Alerts | ⑦ Help

Quick Search: [ ] within [All Full-text Sources ▽] [Go] ⑦ Search Tips

results **1 - 13**

13 Articles Found

pub-date > 1991 and pub-date < 2005 and wire harness w/15 design***

Edit Search | Save Search | Save as Search Alert [ ] [Search Withi]

Article List | Partial Abstracts | Full Abstracts

⌐ [display checked docs] [✉ e-mail articles] [⤷ export citations]   Sort By: [Date ▽] [Go]

1. ☐ **A material and gauge thickness sensitivity analysis on the NVH and crashworthiness of automotive instrument panel support** • ARTICLE
Thin-Walled Structures, Volume 41, Issue 11, November 2003, Pages 1005-1018
K. P. Lam, K. Behdinan and W. L. Cleghorn
SummaryPlus | Full Text + Links | PDF (392 K)

2. ☐ **Design for Postponement** • REVIEW ARTICLE
Handbooks in Operations Research and Management Science, Volume 11, 2003, Pages 199-226
Jayashankar M. Swaminathan and Hau L. Lee
Abstract

3. ☐ **Unexpected behavior of a flexible solar array at retraction under microgravity** • ARTICLE
Acta Astronautica, Volume 50, Issue 11, June 2002, Pages 681-689
Ken Higuchi, M. C. Natori and Masato Abe
SummaryPlus | Full Text + Links | PDF (505 K)

4. ☐ **Challenges in the design of a RGB LED display for indoor applications** • ARTICLE
Synthetic Metals, Volume 122, Issue 1, 1 May 2001, Pages 215-219
Francis Nguyen
SummaryPlus | Full Text + Links | PDF (540 K)

5. ☐ **Supply networks and complex adaptive systems: control versus emergence** • SHORT COMMUNICATION
Journal of Operations Management, Volume 19, Issue 3, May 2001, Pages 351-366
Thomas Y. Choi, Kevin J. Dooley and Manus Rungtusanatham
SummaryPlus | Full Text + Links | PDF (123 K)

6. ☐
The effect of "front-loading" problem-solving on product development performance • ARTICLE
Journal of Product Innovation Management, Volume 17, Issue 2, March 2000, Pages 128-142

Stefan Thomke and Takahiro Fujimoto
Abstract

---

7. □ **Performance of the XRS/ASTRO-E engineering model ADR** • ARTICLE
Cryogenics, Volume 39, Issue 4, April 1999, Pages 399-404
Aristides T. Serlemitsos, Marcelino SanSebastian, Evan S. Kunes and Jason Behr
SummaryPlus | Full Text + Links | PDF (475 K)

---

8. □ **Feature-based cost estimation for packaging products using neural networks** •
ARTICLE
Computers in Industry, Volume 32, Issue 1, 5 December 1996, Pages 95-113
Y. F. Zhang, J. Y. H. Fuh and W. T. Chan
Abstract | Abstract + References | PDF (1382 K)

---

9. □ **The changing boundaries of system companies** • ARTICLE
International Business Review, Volume 5, Issue 6, December 1996, Pages 539-560
Andrea Bonaccorsi, Fabio Pammolli and Simone Tani
Abstract | Abstract + References | PDF (1478 K)

---

10. □ **Activity-based costing model for joint products** • ARTICLE
Computers & Industrial Engineering, Volume 31, Issues 3-4, December 1996,
Pages 725-729
Wen-Hsien Tsai
Abstract | Abstract + References | PDF (394 K)

---

11. □ **Product design for manufacture and assembly** • ARTICLE
Computer-Aided Design, Volume 26, Issue 7, July 1994, Pages 505-520
Geoffrey Boothroyd
Abstract

---

12. □ **Activity-based cost tables to support wire harness design** • ARTICLE
International Journal of Production Economics, Volume 29, Issue 3, May 1993,
Pages 271-289
N. S. Ong
Abstract

---

13. □ **Design of a spaceworthy adiabatic demagnetization refrigerator** • ARTICLE
Cryogenics, Volume 32, Issue 2, 1992, Pages 117-121
A. T. Serlemitsos, M. SanSebastian and E. Kunes
Abstract

---

13 Articles Found

pub-date > 1991 and pub-date < 2005 and wire harness w/15 design***

Edit Search | Save Search | Save as Search Alert

results **1 - 13**

[Home] [Search] [Journals] [Books] [Abstract Databases] [My Profile] [Alerts]   ⑦ Help

Contact Us | Terms & Conditions | Privacy Policy

WEST Search History

| Hide Items | Restore | Clear | Cancel |

DATE: Friday, June 02, 2006

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ	
☐	L3	L2 and layout	13
☐	L2	(wire harness with design$) and (electrical same system?)	78
☐	L1	ash-rafzadeh.in.	1

END OF SEARCH HISTORY

Hit List

First Hit | Clear | | Generate Collection | | Print | | Fwd Refs | | Bkwd Refs |
| Generate OACS |

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 20050183052 A1

Using default format because multiple data bases are involved.

L1: Entry 1 of 1   File: PGPB   Aug 18, 2005

PGPUB-DOCUMENT-NUMBER: 20050183052
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050183052 A1

TITLE: Computer-implemented design tool for synchronizing mechanical and electrical
wire harness designs

PUBLICATION-DATE: August 18, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Ash-Rafzadeh, Armand R.	Northville	MI	US

US-CL-CURRENT: 716/8

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

| Clear | | Generate Collection | | Print | | Fwd Refs | | Bkwd Refs | | Generate OACS |

Term	Documents
ASH-RAFZADEH	1
ASH-RAFZADEHS	0
ASH-RAFZADEH.IN..PGPB,USPT.	1
(ASH-RAFZADEH.IN.).PGPB,USPT.	1

Display Format: |- | | Change Format |

Previous Page   Next Page   Go to Doc#

Hit List

Search Results - Record(s) 1 through 13 of 13 returned.

☐ 1. Document ID: US 20060012969 A1

Using default format because multiple data bases are involved.

```
    L3: Entry 1 of 13                    File: PGPB              Jan 19, 2006

PGPUB-DOCUMENT-NUMBER: 20060012969
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060012969 A1


TITLE: Conforming shielded form for electronic component assemblies and methods for
making and using same


PUBLICATION-DATE: January 19, 2006


INVENTOR-INFORMATION:
NAME                                 CITY            STATE        COUNTRY
Bachman; Bruce                       Bonita          CA           US


US-CL-CURRENT: 361/816; 174/378, 361/818
```

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 2. Document ID: US 20050183052 A1

```
    L3: Entry 2 of 13                    File: PGPB              Aug 18, 2005

PGPUB-DOCUMENT-NUMBER: 20050183052
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050183052 A1


TITLE: Computer-implemented design tool for synchronizing mechanical and electrical
wire harness designs


PUBLICATION-DATE: August 18, 2005


INVENTOR-INFORMATION:
NAME                                 CITY            STATE        COUNTRY
Ash-Rafzadeh, Armand R.              Northville      MI           US


US-CL-CURRENT: 716/8
```

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 3.   Document ID: US 20050156028 A1

L3: Entry 3 of 13   File: PGPB   Jul 21, 2005

PGPUB-DOCUMENT-NUMBER: 20050156028
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050156028 A1

TITLE: Method and apparatus for controlling rented or leased or loaned

PUBLICATION-DATE: July 21, 2005

INVENTOR-INFORMATION:
NAME   CITY   STATE   COUNTRY
Chirnomas, Munroe   Morris Twp.   NJ   US

US-CL-CURRENT: 235/381

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 4.   Document ID: US 20040186620 A1

L3: Entry 4 of 13   File: PGPB   Sep 23, 2004

PGPUB-DOCUMENT-NUMBER: 20040186620
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040186620 A1

TITLE: Method and apparatus for controlling rented or leased or loaned equipment

PUBLICATION-DATE: September 23, 2004

INVENTOR-INFORMATION:
NAME   CITY   STATE   COUNTRY
Chirnomas, Munroe   Morris Township   NJ   US

US-CL-CURRENT: 700/231

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 5.   Document ID: US 20030016519 A1

L3: Entry 5 of 13   File: PGPB   Jan 23, 2003

PGPUB-DOCUMENT-NUMBER: 20030016519
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030016519 A1

TITLE: Conforming shielded form for electronic component assemblies and methods for

making and using same

PUBLICATION-DATE: January 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Bachman, Bruce	Bonita	CA	US

US-CL-CURRENT: 361/818

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 6.   Document ID: US 7013558 B2

L3: Entry 6 of 13   File: USPT   Mar 21, 2006

US-PAT-NO: 7013558
DOCUMENT-IDENTIFIER: US 7013558 B2

TITLE: Method for shielding an electronic component

DATE-ISSUED: March 21, 2006

PRIOR-PUBLICATION:

DOC-ID	DATE
US 20030016519 A1	January 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bachman; Bruce	Bonita	CA		US

US-CL-CURRENT: 29/832; 174/378, 29/527.5, 29/592.1, 29/840, 29/841, 361/736

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

☐ 7.   Document ID: US 6917853 B2

L3: Entry 7 of 13   File: USPT   Jul 12, 2005

US-PAT-NO: 6917853
DOCUMENT-IDENTIFIER: US 6917853 B2

TITLE: Method and apparatus for controlling rented or leased or loaned equipment

DATE-ISSUED: July 12, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chirnomas; Munroe	Morris Township	NJ	07960	

US-CL-CURRENT: 700/<u>244</u>; 700/<u>237</u>, 700/<u>241</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

□ 8.   Document ID: US 6666190 B1

L3: Entry 8 of 13   File: USPT   Dec 23, 2003

US-PAT-NO: 6666190
DOCUMENT-IDENTIFIER: US 6666190 B1

TITLE: Integrated fuel delivery and electrical connection for electronic fuel injectors

DATE-ISSUED: December 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
DiMaria; Anthony Frank	Dearborn	MI		
Gubing, III; William Francis	Canton	MI		
Kunitz; David Walter	Dexter	MI		

US-CL-CURRENT: 123/<u>470</u>; 123/<u>456</u>, 439/<u>76.1</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

□ 9.   Document ID: US 6483719 B1

L3: Entry 9 of 13   File: USPT   Nov 19, 2002

US-PAT-NO: 6483719
DOCUMENT-IDENTIFIER: US 6483719 B1

TITLE: Conforming shielded form for electronic component assemblies

DATE-ISSUED: November 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bachman; Bruce	Bonita	CA		

US-CL-CURRENT: 361/<u>816</u>; 174/<u>378</u>, 252/<u>500</u>, 361/<u>752</u>, 361/<u>800</u>, 455/<u>300</u>

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D |

□ 10.   Document ID: US 6249060 B1

L3: Entry 10 of 13   File: USPT   Jun 19, 2001

US-PAT-NO: 6249060
DOCUMENT-IDENTIFIER: US 6249060 B1

TITLE: Multiplexed cabling system for a vehicle

DATE-ISSUED: June 19, 2001

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Osha; Jonathan P.   Seabrook   TX   77586

US-CL-CURRENT: 307/10.1; 307/9.1

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   11.   Document ID: US 6051782 A
L3: Entry 11 of 13   File: USPT   Apr 18, 2000

US-PAT-NO: 6051782
DOCUMENT-IDENTIFIER: US 6051782 A

TITLE: Conductor layout for electrical junction box

DATE-ISSUED: April 18, 2000

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Wagner; Brian L.   Ypsilanti   MI

US-CL-CURRENT: 174/541; 174/59, 174/71B, 174/72A, 174/72B, 174/99B

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐   12.   Document ID: US 5153839 A
L3: Entry 12 of 13   File: USPT   Oct 6, 1992

US-PAT-NO: 5153839
DOCUMENT-IDENTIFIER: US 5153839 A
** See image for Certificate of Correction **

TITLE: Wire harness manufacturing system

DATE-ISSUED: October 6, 1992

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Cross; Dan A.   Seattle   WA

US-CL-CURRENT: 700/112; 29/33M, 29/564.1, 29/755

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

☐ 13.   Document ID: US 3842496 A

L3: Entry 13 of 13   File: USPT   Oct 22, 1974

US-PAT-NO: 3842496
DOCUMENT-IDENTIFIER: US 3842496 A

TITLE: METHOD AND APPARATUS FOR SEMIAUTOMATICALLY MANUFACTURING ELECTRICAL WIRE HARNESS

DATE-ISSUED: October 22, 1974

INVENTOR-INFORMATION:
NAME   CITY   STATE   ZIP CODE   COUNTRY
Mercer; Paul W.   Bellevue   WA

US-CL-CURRENT: 29/867; 140/71R, 174/72A, 29/564.6, 29/701, 29/711, 29/714, 29/748, 29/755

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De |

| Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS |

Term	Documents
LAYOUT	172049
LAYOUTS	24382
(2 AND LAYOUT).PGPB,USPT.	13
(L2 AND LAYOUT).PGPB,USPT.	13

Display Format: | - | Change Format

Previous Page   Next Page   Go to Doc#